Remarks/Arguments:

Claims 1-5, 7, 9-21, 23-26, 33 and 34 are pending in the application. Claims 1, 9-11, 16-18, 25-26 and 33-34 are rejected. Claims 2-5, 7, 14, 15, 19-21, 23 and 24 are withdrawn by the Examiner. Claims 9, 16, 25 and 34 have been amended. No new matter has been added. Applicants acknowledge with appreciation the indication that claims 12-13 would be allowable if rewritten in independent form. In view of the following, Applicants believe that such amendments are not necessary.

On page 6, the Official Action objects to claims 9, 10-13, 16-17 and 25-26 because they are dependent on non-elected claims. Thus, Applicants have amended the dependency of claims 9, 16 and 25 to depend on elected claims. Withdrawal of the objection is respectfully requested.

On page 2, the Official Action rejects claims 1, 9-11, 16-18, 25-26 and 33-34 under 35 U.S.C. § 103(a) as being unpatentable over Matsumi (U.S. Patent No. 6,038,094) in view of Shinohara (U.S. Patent No. 5,740,306) and further in view of Inazumi (U.S. Patent No. 6,493,362). It is respectfully submitted, however, that the claims are patentable over the art of record for at least the reasons set forth below.

Applicants' invention, as recited by claim 1, includes a feature which is neither disclosed nor suggested by the art of record, namely:

> **data rate detecting means of detecting a data rate of the received bit stream by counting a number of packets received by said inputting means over a predetermined time, the predetermined time being a time taken by said recording means to record data ...**

Claim 1 relates to determining the data rate based on counting packets of data of known size over a known time period. Based on the number of packets counted, the size of the packets and the length of the time period, the data rate is determined. This feature is at least supported in Applicants' specification on page 24, line 20 to page 25, line 10, and furthermore on page 34, line 20 to page 35, line 8. No new matter has been added.

On page 4, the Official Action states that Inazumi discloses detecting data rate by counting the number of packets over a predetermined time. Applicants, however, respectfully disagree. In Column 9, lines 35-65, Inazumi teaches that the recording of reproducing bit rate is set based on the internal clock signal ("*here, the recording of reproducing bit rate R of the data recording/reproducing unit 100 is set based on the internal clock signal outputted from the frequency divider 25 to the PCR generating section 17*"). Thus, even though Inazumi counts the number of packets by packet counter 16, the bit rate is not determined by the counted number of packets. The bit rate in Inazumi is determined based on an internal clock signal unrelated to the number of counted packets. The internal clock oscillator 24 and frequency divider 25 which dictate the bit rate, are also shown in Inazumi's Fig. 3 (they are not connected to the packet counter).

Applicants' claim 1 is different than the art of record, because the data rate is computed based on the counted number of packets ("*data rate detecting means of detecting a data rate of the received bit stream by counting a number of packets received by said inputting means over a predetermined time, the predetermined time being a time taken by said recording means to record data ...*"). As shown in Fig. 1, for example, packet counter section 3 counts the number of packets and outputs the counted number of packets to system controller 6. Based on the counted number of packets, the data rate is then determined. This feature is at least supported in Applicants' specification page 24, line 20 to page 25, line 10 ("*packet counter section 3 counts the number of packets in the input bit stream at intervals of predetermined time periods ... the packets are of the fix length type ...*"). Determination of the bit rate is at least shown in Fig. 5B where bit rate calculating circuit 20 utilizes the packet counter value to determine the bit rate. For example, as disclosed in Applicants' specification page 34, line 20 to page 35, line 10, bit rate calculating circuit 20 is disclosed ("*Bit rate calculating circuit 20 calculates the bit rate of input packets from the packet number. On the output of the counter value holding circuit 17 is N packets, the time period for one track is a time T seconds and the amount of data per packet is D bytes, for example, the recording rate R is calculated by an expression indicated by R = (D X 8 X N)/T.*"). Thus, based on the counted number of data packets N, the data bit rate R is able to be computed. Accordingly, for the reasons set forth above, claim 1 is patentable over the art of record. Withdrawal of the rejection and allowance of claim 1 is respectfully requested.

Independent claims 18, 33 and 34 have similar features to claim 1. Thus, these claims are also patentable over the art of record for at least the reasons set forth above with respect to claim 1.

Dependent claims 9-11, 16-17 and 25-26 include all the features of the claims from which they depend. Thus, these claims are also patentable over the art of record for at least the reasons set forth above.

In view of the amendments and arguments set forth above, the above-identified application is in condition for allowance which action is respectfully requested.

Respectfully submitted,

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